UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte STAN W. BOWLIN

Appeal No. 2005-1612
Application No. 09/675,974

ON BRIEF

Before JERRY SMITH, BARRY, and SAADAT, *Administrative Patent Judges.*
BARRY, *Administrative Patent Judge.*

A patent examiner rejected claims 1-19. The appellant appeals therefrom under 35 U.S.C. § 134(a). We affirm-in-part.

I. BACKGROUND

The invention at issue on appeal is a testing instrument. In testing computer networks, an efficient use of testing capabilities is needed to maximize analysis abilities and minimize hardware requirements. (Spec. at 1.) Figure 1 of the appellant's specification shows a network testing device 10. The device connects to a network 12 via a media access controller ("MAC") 14. A bus 16 connects the MAC to a synchronous dynamic random access memory ("SDRAM") 18 and a digital signal

processor ("DSP") 20. (*Id.* at 2.) According to the appellant, heretofore, data from the MAC were read by the DSP via the bus, and, if the data were to be stored, the DSP would write the data to the SDRAM "in a separate bus transfer operation." (*Id.* at 2-3.)

When the appellant's invention retrieves data from the MAC, in contrast, it simultaneously writes the data to the DSP and the SDRAM. If the DSP determines that the data are to be saved, it updates address pointers to the memory to select a next position in the SDRAM for future data. If the DSP determines that the data are not to be saved, it leaves the address pointers set at the starting point of the prior write to memory. Consequently, the next data provided from the MAC are written "over" the previous data that was not to be saved. According to the appellant, therefore, data received from the MAC need only travel the bus once, thereby speeding operations. (*Id.* at 3.)

A further understanding of the invention can be achieved by reading the following claims.

> 1. A method for transferring a unit of data on a bus from a source to at least two destinations substantially simultaneously, comprising the steps of:
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> supplying said unit of data from the source to first of said at least two destinations as a read data operation; and

supplying said unit of data to a second of said at least two destinations as a write operation.

8. An apparatus for transferring received data in discrete units from a network, comprising:

a bus;

a media access controller for putting ones of discrete units of the received data from the network onto said bus;

a microprocessor for reading the ones of discrete units of data from said bus;

a memory for writing the ones of discrete units of data from said bus into said memory; and

a timing controller for controlling said media access controller, said microprocessor and said memory to have said media access controller write selected ones of discrete units of the data to the bus, said memory write said selected ones of discrete units of the data to said memory and said microprocessor read said selected ones of discrete units of the data substantially simultaneously.

9. An apparatus for transferring data, comprising:

a bus;

a FIFO data source connected to said bus for putting data onto said bus;

a microprocessor connected to said bus for reading the data from said bus;

a memory connected to said bus for writing the data from said bus into said memory; and

a timing controller connected to said FIFO data source, said microprocessor and said memory for controlling said FIFO data source, said microprocessor and said memory to have said FIFO data source put the data onto the bus, and for a selected quantity of data, have said memory write the selected quantity of data to said memory and said microprocessor read the selected quantity of data substantially simultaneously.

10. The apparatus for transferring data according to claim 9, wherein said FIFO device [sic] is a media access controller.

11. The apparatus for transferring data according to claim 9, wherein said apparatus is a network test instrument and said FIFO device [sic] is a media access controller.

16. A method for operating a network test instrument to transfer data on a bus within said network test instrument from a media access controller at least to a processor and to a memory, separate from said processor, comprising the steps of:

supplying said data from the media access controller to said processor as a read data operation performed by said processor; and

supplying said data to said memory as a write operation,

wherein said step of supplying data to said processor and said step of supplying data to said memory are accomplished substantially simultaneously with use of the same transfer of said data on said bus.

Claims 10 and 11 stand rejected under 35 U.S.C. § 112, ¶ 2, as indefinite. Claims 1-19 stand rejected under 35 U.S.C. § 112, ¶ 1, as non-enabled. Claims 1, 4-8, 12, 14-16, and 19 stand rejected under 35 U.S.C. § 103(a) as obvious over the

appellant's admitted prior art ("AAPA") and U.S. Patent No. 5,073,851 ("Masterson"). Claims 2, 3, 9-11, and 13 stand rejected under § 103(a) as obvious over AAPA; Masterson; and U.S. Patent No. 5,379,289 ("DeSouza"). Claims 17 and 18 stand rejected under § 103(a) as obvious over AAPA; Masterson; and an article entitled "Circuit for Tracing Branch Instructions" ("IBM-TDB").

II. OPINION

When claims have been rejected under the first and second paragraphs of 35 U.S.C. § 112, analysis "should begin with the determination of whether the claims satisfy the requirements of the second paragraph." *In re Moore*, 439 F.2d 1232, 1235, 169 USPQ 236, 238 (CCPA 1971). Accordingly, our opinion addresses the rejections in the following order:

- indefiniteness rejection of claims 10 and 11
- non-enablement rejection of claims 1-19
- obviousness rejections of claims 1-17 and 19
- obviousness rejection of claim 18.

A. INDEFINITENESS REJECTION OF CLAIMS 10 AND 11

"Rather than reiterate the positions of the examiner or the appellant *in toto*, we focus on the point of contention therebetween." *Ex parte Kaysen*, No. 2003-0553, 2004 WL 1697755, at *2 (Bd.Pat.App & Int. 2004 Feb. 10, 2005). Observing that "[t]he

claims recite respectively the limitation 'said FIFO device' in line 1 of the claim 10, and in line 3 of the claim 11," (Examiner's Answer at 5), the examiner asserts, "There is insufficient antecedent basis for this limitation in the claim." (*Id.*) Admitting that "it is clear that claims 10 and 11 had typographical errors in them," (Appeal Br.[1] at 10), the appellant "respectfully asks that error be corrected. . . ." (*Id.*) We have no authority, however, to correct errors in claims. The appellant then argues, "Even without correction, it is clear what the claims mean." (*Id.*)

A claim is indefinite "where the language 'said lever' appears in a dependent claim where no such 'lever' has been previously recited in a parent claim to that dependent claim . . . ." *Ex parte Moelands*, 3 USPQ2d 1474, 1476 (Bd.Pat.App. & Int. 1987).

Here, although claims 10 and 11 each includes the language "said FIFO device," it is uncontested that no such "FIFO **device**" has been previously recited therein or in claim 9, from which claims 10 and 11 depend. Because the claims lack antecedent basis for "said FIFO device," we are unpersuaded that one skilled in the art would

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[1]We rely on and refer to the "New" Appeal Brief, filed on July 14, 2004, in lieu of the original appeal brief, filed on April 15, 2004, because the latter was defective. (Paper No. 13.) The original appeal brief was not considered in deciding this appeal.

understand the bounds of claims 10 and 11 when read in light of the specification. Therefore, we affirm the indefiniteness rejection of claims 10 and 11.

B. NON-ENABLEMENT REJECTION OF CLAIMS 1-19

Observing that "the Appellant recites the limitation 'transferring a unit of data on a bus from a source to at least two destinations substantially simultaneously,' in the claim[s]," (Examiner's Answer at 20), the examiner asserts, "the Appellant fails to explain how to substantially simultaneously transferring data to at least two destination with separate operation signals, i.e., read at T4/5 and write at T7 operations in Fig. 2." (*Id.* at 23.) The appellant argues, "The READ command at time T4/5 is merely a command to set the DSP chip up for a read operation. The reading does not take place until some time slices later, WHEN THE DATA IS [sic] ACTUALLY ON THE BUS." (Reply Br. at 4.)

"[T]he PTO bears an initial burden of setting forth a reasonable explanation . . . why it believes that the scope of protection provided by that claim is not adequately enabled by the description of the invention provided in the specification of the application. . . ." *In re Wright*, 999 F.2d 1557, 1561-62, 27 USPQ2d 1510, 1513 (Fed. Cir. 1993) (citing *In re Marzocchi*, 439 F.2d 220, 223-24, 169 USPQ 367, 369-70 (CCPA 1971)). "The test of enablement is whether one reasonably skilled in the art

could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation." *U.S. v. Telectronics, Inc.*, 857 F.2d 778, 785, 8 USPQ2d 1217, 1223 (Fed. Cir. 1988) (citing *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1384, 231 USPQ 81, 94 (Fed.Cir.1986)).

Here, independent claim 16 recites in pertinent part the following limitations: "said step of supplying data to said processor and said step of supplying data to said memory are accomplished **substantially simultaneously** with use of the same transfer of said data on said bus." (Emphasis added.) The other independent claims recite similar limitations.

Turning to the rest of the appellant's specification, "FIG. 2 is a timing diagram of operations according to the invention." (Spec. at 2.) As shown therein, upon "an indication that data is available in . . . the MAC, the Dsp-command line is set to ACTIVE during the last half of clock cycle 1 . . . for a duration of one cycle." (*Id.* at 4.) "In the middle of clock cycle 4, . . . the Dsp-command is set to READ (indicating a read) . . . for [a] 1 clock cycle duration." (*Id.*) "Soon after cycle 6 starts, the MAC Rx-Data will begin on line 34 carrying the first word of data W1, the data W1 remaining until the end of cycle 7. At the start of cycle 7, Sdram-command is set to WRITE for one clock

[cycle]." (*Id.*) "The Rx-Data line will subsequently carry valid data from the MAC for next words W2, W3, W4, W5,W6 and W7 during the last half of clocks 9-13, respectively." (*Id.* at 5.)

It is uncontested that "data cannot start being read by the DSP from the bus before it appears on the bus." (Appeal Br. at 7.) Because Figure 2 shows that these data, viz., W1-W7, do not appear on the bus until "[s]oon after cycle 6 starts," (Spec. at 2), we are persuaded that the READ command activated in the middle of clock cycle 4 "is merely a command to set the DSP chip up for a read operation." (Reply Br. at 4.) We are further persuaded that the reading does not take place until some time slices later, when the data are actually on the bus. (*Id.*) We agree with the appellant that requiring the READ signal "to be enabled before the data to be read are present," does not make the specification non-enabling." (Appeal Br. at 8.) Therefore, we reverse the non-enablement rejection of claims 1-19.

C. OBVIOUSNESS REJECTIONS OF CLAIMS 1-17 AND 19

"[T]o assure separate review by the Board of individual claims within each group of claims subject to a common ground of rejection, an appellant's brief to the Board must contain a clear statement for each rejection: (a) asserting that the patentability of claims within the group of claims subject to this rejection do not stand or fall together,

and (b) identifying which individual claim or claims within the group are separately patentable and the reasons why the examiner's rejection should not be sustained." *In re McDaniel*, 293 F.3d 1379, 1383, 63 USPQ2d 1462, 1465 (Fed. Cir. 2002) (citing 37 C.F.R. §1.192(c)(7) (2001)). "If the brief fails to meet either requirement, the Board is free to select a single claim from each group of claims subject to a common ground of rejection as representative of all claims in that group and to decide the appeal of that rejection based solely on the selected representative claim." *Id.*, 63 USPQ2d at 1465.

Here, the appellant stipulates that claims 1, 4-7, 12, and 19 *inter alia* "stand or fall" together. (Appeal Br. at 6.) We select claim 1 from the group as representative of the claims therein.

The examiner finds, "AAPA discloses . . . supplying a second unit of data from said source (i.e., MAC) to first of said at least two destinations (i.e., DSP) as a read data operation (See page 2, line 35), and supplying said first unit of data to a second of said at least two destinations (i.e., SDRAM) as a write operation (See page 3, line 2)." (Examiner's Answer at 6.) He further finds, "Masterson discloses an apparatus and method for improved caching in a computer system, wherein a first and second units of data transferring would been substantially simultaneously performed ([s]ee claim 1 and

col. 5, lines 57-60,. i.e., a read operation of a first unit of data (e.g., byte 2) is substantially simultaneously overlapped with a write operation of a second unit of data (i.e., byte 1))." (Examiner's Answer at 6.) The appellant argues, "In the prior art, at time T1, there is only a read, no write. But then, at time T2, there are both read and writes, but the read and writes do not involve a unit of data — they involve separate data items." (Appeal Br. at 11-12.)

In addressing the point of contention, the Board conducts a two-step analysis. First, we construe claims at issue to determine their scope. Second, we determine whether the construed claims would have been obvious.

1. Claim Construction

"Analysis begins with a key legal question — *what* is the invention *claimed*?" *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). In answering the question, "the Board must give claims their broadest reasonable construction. . . ." *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1668 (Fed. Cir. 2000). "Moreover, limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)).

"Generally, . . . the preamble does not limit the claims." *DeGeorge v. Bernier*, 768 F.2d 1318, 1322 n.3, 226 USPQ 758, 761 n.3 (Fed. Cir. 1985). In particular, "[t]he preamble of a claim does not limit the scope of the claim when it merely states a purpose or intended use of the invention." *In re Paulsen*, 30 F.3d 1475, 1479, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994) (citing *DeGeorge*, 768 F.2d at 1322 n.3, 226 USPQ at 761 n.3). "Where . . . the effect of the words [in the preamble] is at best ambiguous . . . a compelling reason must exist before the language can be given weight." *Arshal v. United States*, 621 F.2d 421, 430-31, 208 USPQ 397, 406-07 (Ct. Cl. 1980) (citing *In re de Castelet*, 562 F.2d 1236, 1244 n.6, 195 USPQ 439, 447 n.6 (CCPA 1977)).

Here, claim 1 recites in pertinent part the following limitations:

> A method for transferring a unit of data on a bus from a source to at least two destinations *substantially simultaneously*, comprising the steps of:
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> supplying said unit of data from the source to first of said at least two destinations as a read data operation; and
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> supplying said unit of data to a second of said at least two destinations as a write operation.

(Emphasis added.) In contrast to claims 8, 9, and 16, the phrase "substantially simultaneously" is mentioned only in the preamble of the representative claim, and its mention merely states a purpose or intended use of the claimed method. The body of

the claim neither repeats nor references the phrase. Instead, the body specifies a read operation and a write operation, with no requirement that the operations be performed "substantially simultaneously." Because the language in the body of claim 1 standing alone is clear and unambiguous, we find no compelling reason to give the phrase "substantially simultaneously" weight.

In contrast, the body of claim 8 recites in pertinent part the following limitations: "for a selected quantity of data, have said memory write the selected quantity of data to said memory and said microprocessor read the selected quantity of data substantially simultaneously." The bodies of independent claims 9 and 16 recite similar limitations. Accordingly, claims 8, 9, and 16 require that the same datum is simultaneously written to a memory and read by a microprocessor.

2. Obviousness Determination

Having determined what subject matter is being claimed, the next inquiry is whether the subject matter would have been obvious. The question of obviousness is "based on underlying factual determinations including . . . what th[e] prior art teaches explicitly and inherently. . . ." *In re Zurko*, 258 F.3d 1379, 1383, 59 USPQ2d 1693, 1696 (Fed. Cir. 2001) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ

459, 467 (1966); *In re Dembiczak*, 175 F.3d 994, 998, 50 USPQ 1614, 1616 (Fed. Cir. 1999); *In re Napier*, 55 F.3d 610, 613, 34 USPQ2d 1782, 1784 (Fed. Cir. 1995)). "'A *prima facie* case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art.'" *In re Bell*, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting *In re Rinehart*, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

Here, as aforementioned, the examiner finds that AAPA discloses supplying a second unit of data from a MAC to a DSP as a read data operation and supplying a first unit of data to a SDRAM as a write operation. (Examiner's Answer at 6.) The AAPA validates that finding by disclosing that "in accordance with the prior art, data received from the MAC would be read by the DSP via the bus, and, if the data was [sic] to be stored, it would be written to the SDRAM via the bus by the DSP. . . ." (Spec. at 2.) Therefore, we affirm the obviousness rejection of claim 1 and of claims 4-7, 12, and 19, which fall therewith.

In addressing claims 2, 3, and 13, the appellant relies on the argument he advanced for claim 1, (Appeal Br. at 14), which we have found unpersuasive. Therefore, we also affirm the obviousness rejection of claim 2, 3, and 13.

The examiner admits that "AAPA does not teach said first and second units of data transferring would been [sic] substantially simultaneously performed." (Examiner's Answer at 6.) As aforementioned, he relies on Masterson ("secondary reference") for that teaching. For its part, the secondary reference "relates to . . . methods and apparatus for improving the speed of operations of a computer system. . . ." Col. 1, ll. 7-9. "FIG. 2 is a block diagram of a computer system constructed in accordance with [Masterson's] invention." Col. 2, ll. 40-41. "The system 30 includes a central processing unit 12, a cache memory 18, and a main memory 15." Col. 3, ll. 65-67.

"[A]s the information in the main memory 15 is accessed using the addresses in main memory 15 furnished by the central processing unit 12, the output is written into the cache memory 18." Col. 5, ll. 52-55. We are unpersuaded, however, that the same datum is simultaneously written to the cache memory 18 and read by the central processing unit 12. To the contrary, the secondary reference "substantially simultaneously overlaps the read access of the main memory 15 and the write access of cache memory 18 such that, for example when byte 2 is being read, byte 1 is being written and when byte 3 is being read, byte 2 is being written, etc. . . ." *Id.* at ll. 57-62.

Furthermore, the examiner does not allege, let alone show, that the addition of DeSouza or IBM_TDB cures the aforementioned deficiency of AAPA and Masterson. Absent a teaching or suggestion that the same datum is substantially simultaneously written to a memory and read by a microprocessor, we are unpersuaded of a *prima facie* case of obviousness. Therefore, we reverse the obviousness rejections of claim 8; of claim 9; of claims 10 and 11, which depend from claim 9; of claim 16; and of claim 17, which depends from claim 16.

D. OBVIOUSNESS REJECTION OF CLAIM 18

The examiner makes the following finding.

> IBM_TDB discloses a tracing test system, wherein determining (i.e., by Branch Detect Circuit in Fig. 1) whether a data (i.e., instruction) currently transferred to a memory (i.e., Trace Memory in Fig. 1) is to be retained before a next data is transferred said memory (See Disclosure Text 2nd paragraph, lines 1-4), and if said data currently transferred is to be retained (i.e., if the current instruction is a branch instruction), modifying a next write address location so that a next data does not overwrite said data currently transferred (See Disclosure Text 2nd paragraph, lines 8-14 and 17-19), and otherwise, if said data currently transferred is not to be retained in said memory, keeping said next data write address as a current data write address value so that said next data is written over said data currently transferred (See Disclosure Text 2nd paragraph, lines 6-8 and 15-16).

(Examiner's Answer at 19.) He then draws the following conclusion.

> [I]t would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method steps of tracing test

> system, as disclosed by IBM_TDB, in said method, as disclosed by AAPA, as modified by Masterson, so as to record said data (i.e., each instruction) operated on a network (i.e., executed by a processor) under test, for the advantage of generating an audit trail that is helpful in system debug (See Disclosure Text, 1st paragraph, lines 1 -3).

(*Id.*) The appellant does not contest the examiner's findings about what IBM_TDB teaches or his motivation for combining the teachings of the references. Instead, the appellant "submit[s] that one would not look to circuits for avoiding filling trace memory when tracing branch instructions in a processor under test when constructing methods and devices such as applicant's, wherein the goal is to speed operations rather than to save memory capacity." (Appeal Br. at 16.)

"Whether a reference in the prior art is 'analogous' is a fact question." *In re Clay*, 966 F.2d 656, 658, 23 USPQ2d 1058, 1060 (Fed. Cir. 1992) (citing *Panduit Corp*, 810 F.2d at 1568 n.9, 1 USPQ2d at 1597 n.9). Two criteria have evolved for answering the question: "(1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the inventor's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the inventor is involved." *Id.* at 658-59, 23 USPQ2d at 1060 (citing *In re Deminski*, 796 F.2d 436, 442, 230 USPQ 313, 315 (Fed. Cir. 1986); *In re Wood*, 599 F.2d 1032, 1036, 202 USPQ 171, 174 (CCPA 1979)).

Here, regarding the first criterion, the appellant states that "[]his invention relates to test instruments. . . ." (Spec. at 1.) For its part, IBM_TDB also relates to test instruments, viz., "[t]racing **test** systems . . . helpful in system debug." Ll. 1-3. Because the inventions of the appellant and the reference are both from the field of testing, we find that IBM_TDB is analogous art. Therefore, we affirm the obviousness rejection of claim 18.

III. CONCLUSION

In summary, the rejection of claims 10 and 11 under 35 U.S.C. § 112, ¶ 2, is affirmed. The rejection of claims 1-19 under 35 U.S.C. § 112, ¶ 1, in contrast, is reversed. The rejections of claims 1, 2-7, 12, 13, 18, and 19 under § 103(a) are affirmed. In contrast, the rejections of claims 8-11, 16, and 17 under § 103(a) are reversed. Although the appellant submits that these claims *inter alia* "are . . . allowable," (Appeal Br. at 15, 16), the Board has no authority to allow claims.

"Any arguments or authorities not included in the brief will be refused consideration by the Board of Patent Appeals and Interferences. . . ." 37 C.F.R. § 1.192(a). Accordingly, our affirmance is based only on the arguments made in the briefs. Any arguments or authorities omitted therefrom are neither before us nor at

issue but are waived. *Cf. In re Watts*, 354 F.3d 1362, 1367, 69 USPQ2d 1453, 1457 (Fed. Cir. 2004) ("[I]t is important that the applicant challenging a decision not be permitted to raise arguments on appeal that were not presented to the Board.")

No time for taking any action connected with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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LANCE LEONARD BARRY
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